PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Warren M. Farnworth

Patent No.: 7,170,361 B1

Issued: January 30, 2007

For: METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES

Attorney Docket No.: 2269-4161US

CERTIFICATE OF MAILING

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March 1, 2007
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Shawnee MacDonald
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REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR APPLICANT'S MISTAKES (37 C.F.R. § 1.323) AND PATENT OFFICE MISTAKES (37 C.F.R. § 1.322)

Attn.: Certificate of Corrections Branch
Commissioner for Patents
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Sir:

It is noted that a combination of Applicant and Patent Office errors appear in this patent of a typographical nature or character and correction thereof does not involve such changes in the patent as would constitute new matter or would require reexamination. A certificate of correction in the form attached hereto is requested.

Please note that an Amendment in Response to Office Action dated April 26, 2004, was filed on July 26, 2004, and an Amendment in Response to Office Action dated January 4, 2006, was filed on April 4, 2006. Both of these amendments included drawing changes and formal drawings that were inadvertently not used by the Patent Office in printing of the patent. Attached are copies of the previously filed amendments and the date-stamped postcards acknowledging

receipt by the PTO in order to provide proof of their filing. We have included replacement formal drawings on the attached PTO/SB/44 with at least one copy being suitable for printing. Applicant has included a check in the amount of $100.00 because Applicant inadvertently failed to file formal drawings of FIGs. 14 and 15.

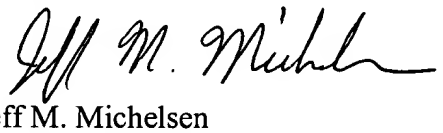
Please send the Certificate to:

Name: Jeff M. Michelsen
Address: TraskBritt
P.O. Box 2550
Salt Lake City, Utah 84110

The fee of $100.00 as required by 37 C.F.R. § 1.20(a) is enclosed.

Attached hereto in duplicate is Form PTO/SB/44 with at least one copy being suitable for printing.

Respectfully submitted,



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Registration No. 50,978
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: March 1, 2007
JMM/csw

Enclosures: PTO/SB/44 in duplicate
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APPLICATION NO : 09/548,942
DATED : January 30, 2007
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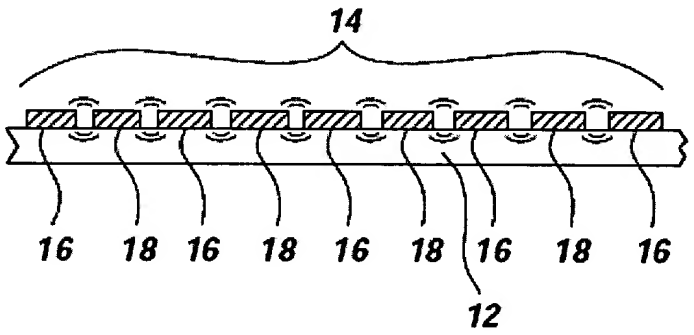

In item (56), "References Cited,"
U.S. PATENT DOCUMENTS,
2nd column, 10th entry:

Delete "6,262,660 B1 * 7/2001 Segale et al. ...257/728" and insert in its place:
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In the drawings:

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In FIG. 2,	replace the informal drawing of FIG. 2 with the formal drawing of FIG. 2
In FIG. 3,	replace the informal drawing of FIG. 3 with the formal drawing of FIG. 3
In FIG. 4,	replace the informal drawing of FIG. 4 with the formal drawing of FIG. 4
In FIG. 5,	replace the informal drawing of FIG. 5 with the formal drawing of FIG 5
In FIG. 11,	replace the drawing of FIG. 12 with FIG. 12 amended on April 4, 2006, by inserting reference numerals --28-- and --29-- (two occurrences each)
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In FIG. 15,	replace the informal drawing of FIG. 15 with the formal drawing of FIG.15

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In the claims:

CLAIM 2, COLUMN 8, LINE 29, change "comprising;" to --comprising:"

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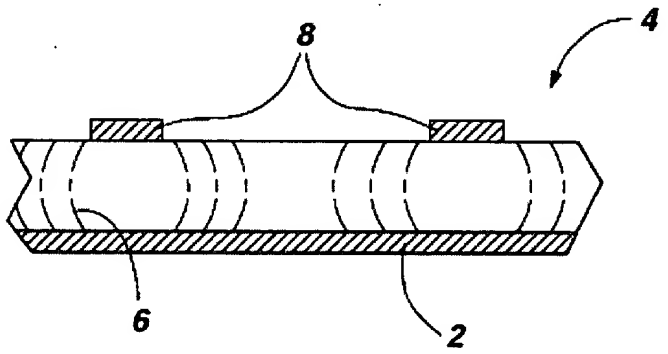

Fig. 1
(PRIOR ART)

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Please replace FIG. 2 with the following replacement figure:

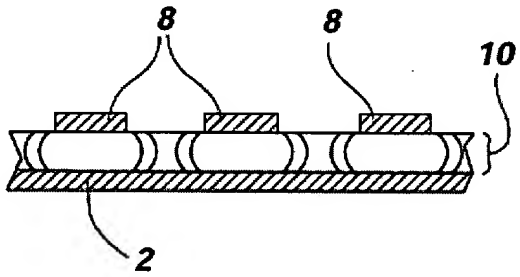

Fig. 2
(PRIOR ART)

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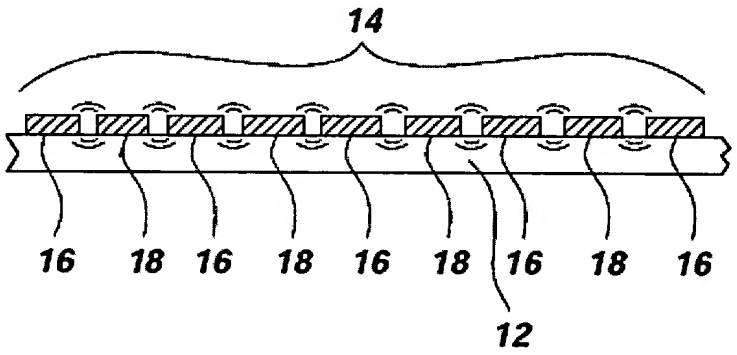

Fig. 3

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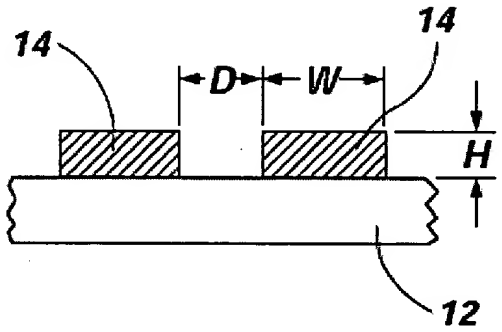

Fig. 4

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Please replace FIG. 5 with the following replacement figure:

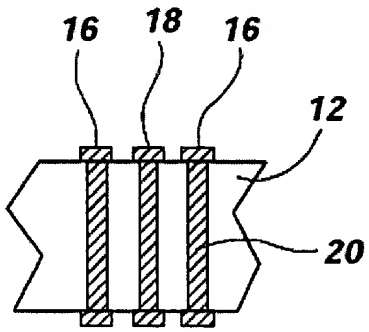

Fig. 5

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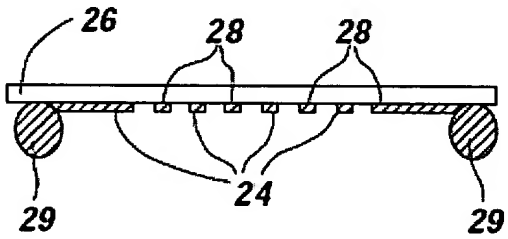

Fig. 11

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Please replace FIG. 12 with the following replacement figure:

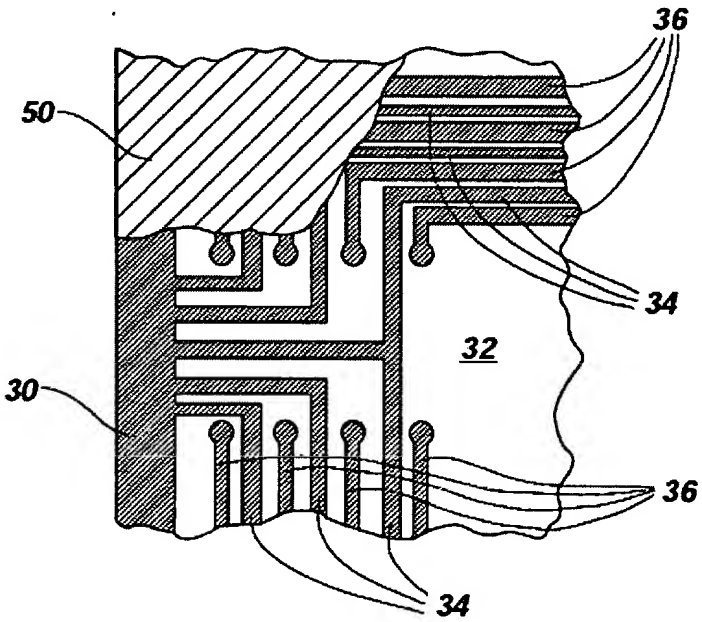

Fig. 12

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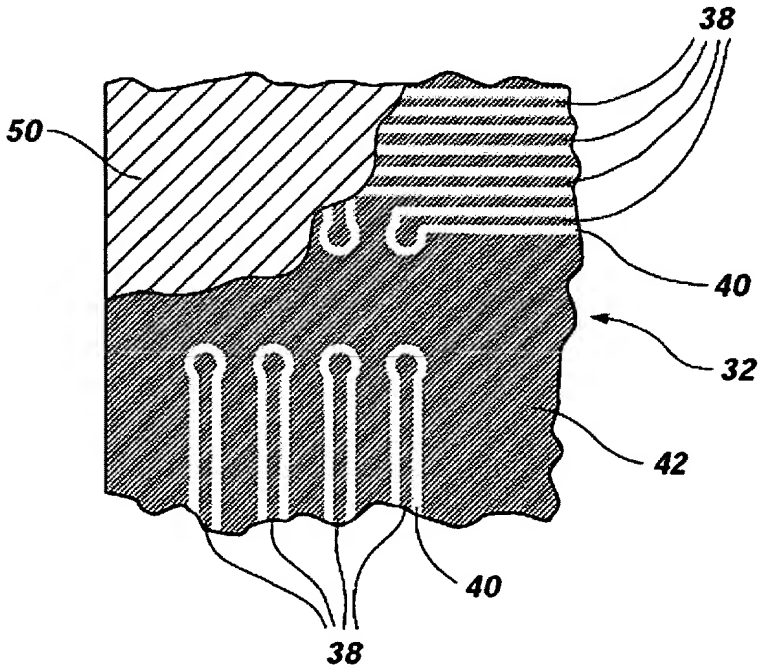

Fig. 13

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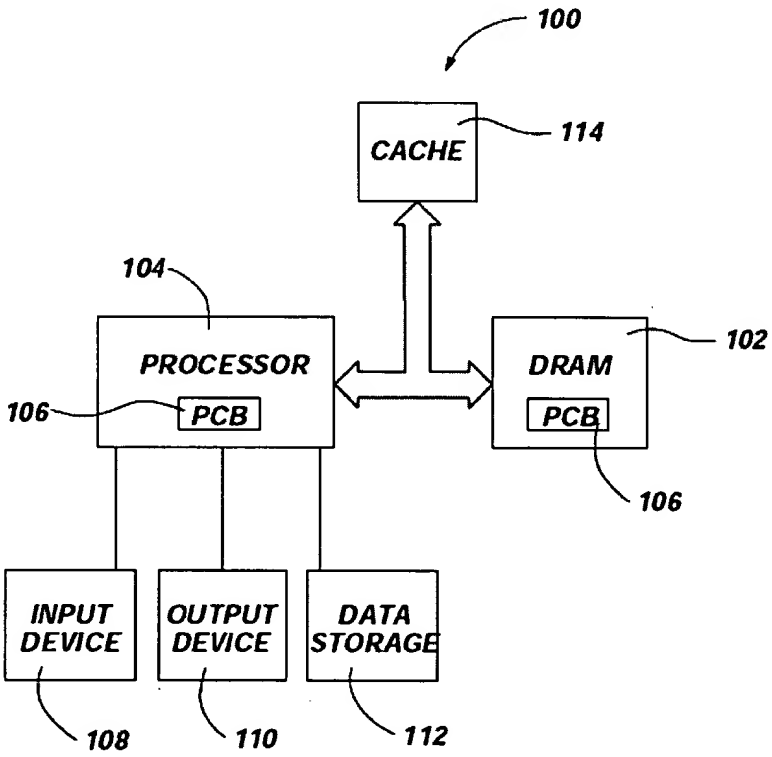

Fig. 14

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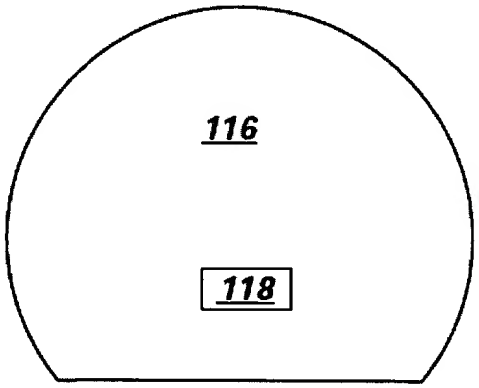

Fig. 15

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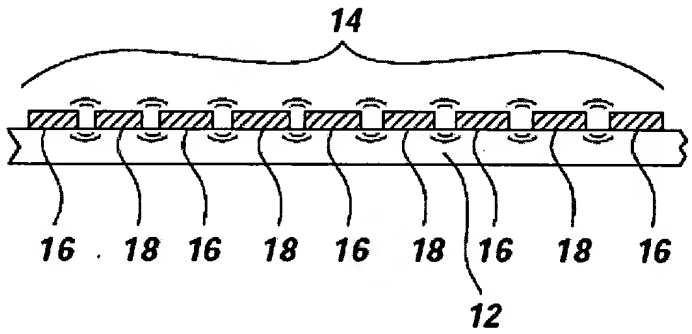

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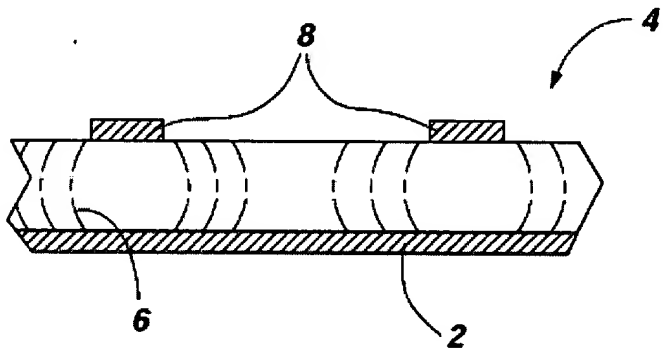

Fig. 1
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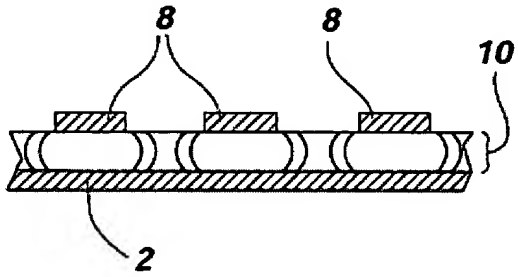

Fig. 2
(PRIOR ART)

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,170,361 B1
APPLICATION NO : 09/548,942
DATED : January 30, 2007
INVENTOR(S) : Warren M. Farnworth

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace FIG. 3 with the following replacement figure:

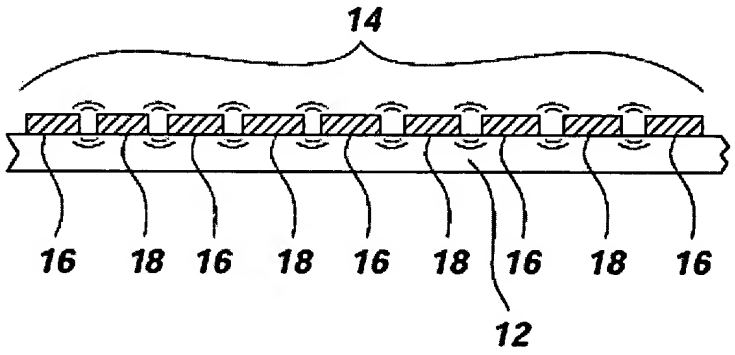

Fig. 3

MAILING ADDRESS OF SENDER:

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INVENTOR(S) : Warren M. Farnworth

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Please replace FIG. 4 with the following replacement figure:

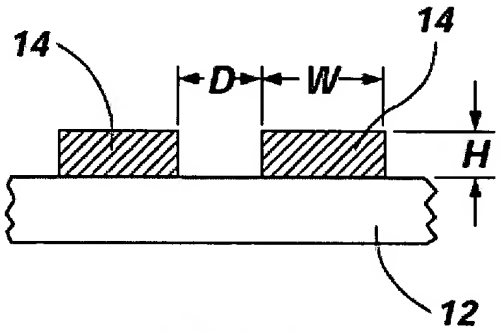

Fig. 4

MAILING ADDRESS OF SENDER:

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INVENTOR(S) : Warren M. Farnworth

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace FIG. 5 with the following replacement figure:

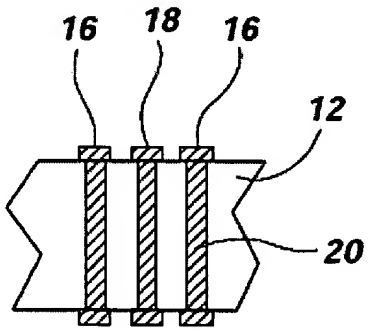

Fig. 5

MAILING ADDRESS OF SENDER:

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DATED : January 30, 2007
INVENTOR(S) : Warren M. Farnworth

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace FIG. 11 with the following replacement figure:

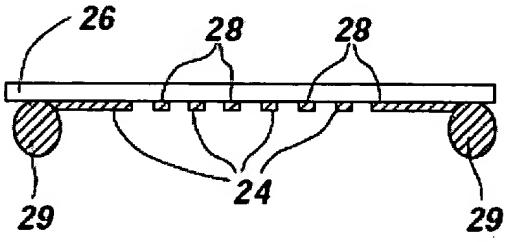

Fig. 11

MAILING ADDRESS OF SENDER:

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INVENTOR(S) : Warren M. Farnworth

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace FIG. 12 with the following replacement figure:

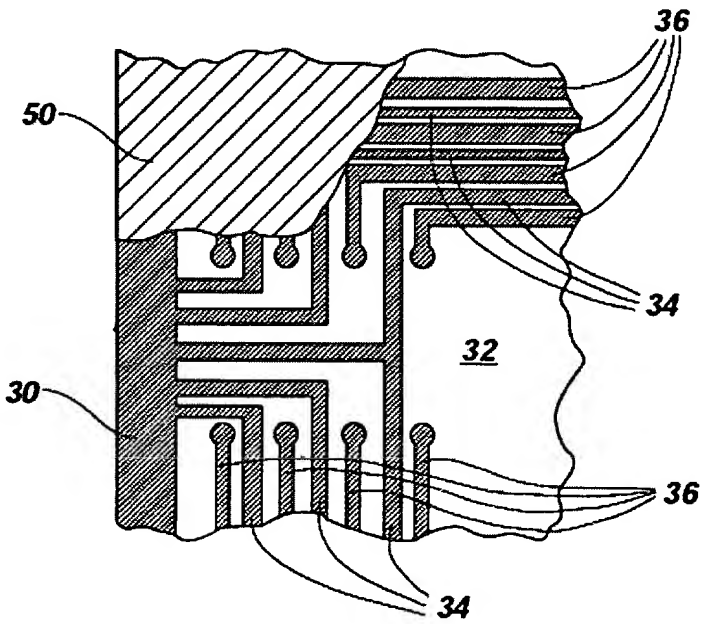

Fig. 12

MAILING ADDRESS OF SENDER:

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DATED : January 30, 2007
INVENTOR(S) : Warren M. Farnworth

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace FIG. 13 with the following replacement figure:

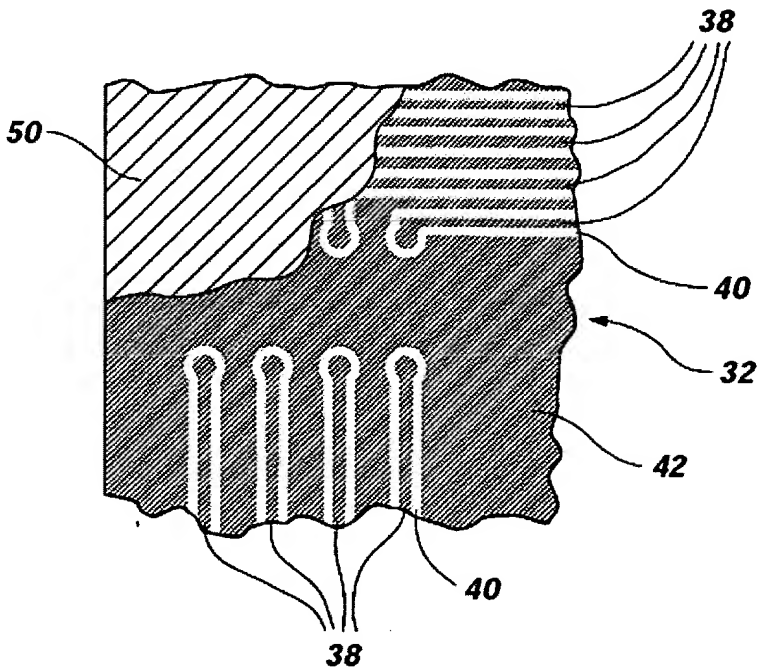

Fig. 13

MAILING ADDRESS OF SENDER:

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DATED : January 30, 2007
INVENTOR(S) : Warren M. Farnworth

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace FIG. 14 with the following replacement figure:

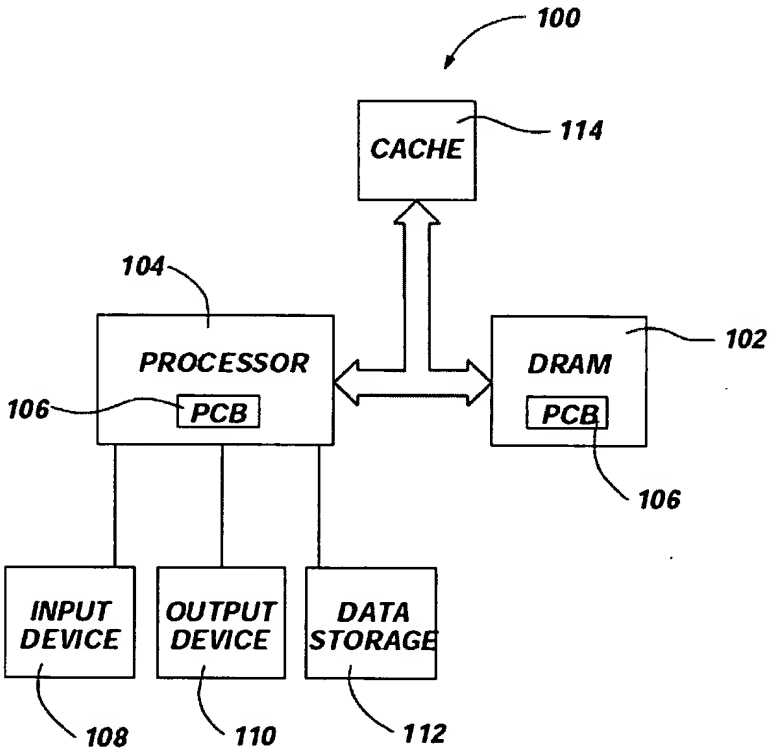

Fig. 14

MAILING ADDRESS OF SENDER:

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PATENT NO : 7,170,361 B1
APPLICATION NO : 09/548,942
DATED : January 30, 2007
INVENTOR(S) : Warren M. Farnworth

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please replace FIG. 15 with the following replacement figure:

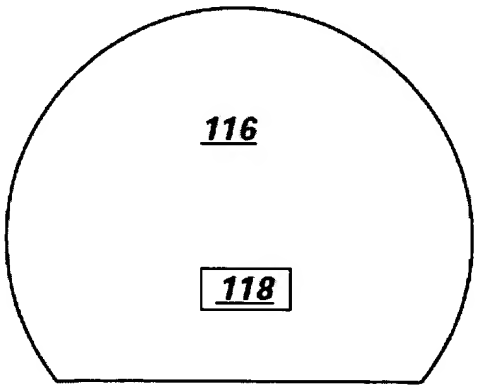

Fig. 15

MAILING ADDRESS OF SENDER:

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THE PATENT & TRADEMARK OFFICE MAILROOM DATE STAMP HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Amendment in response to office action dated April 26, 2004 with Appendices A , B, and C which includes a Substitute Specification and Abstract, Marked-Up Specification and Abstract, and Proposed Drawing Corrections (59 total pages); Check no. 20580 in the amount of $86.00.

Invention:	METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES
Applicant(s):	Warren M. Farnworth
Filing Date:	April 13, 2000
Serial No.:	09/548,942
Date Sent:	July 26, 2004 via first class mail
Docket No.:	2269-4161US
JMM/ljb	

MAR - 9 2005

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Warren M. Farnworth

Serial No.: 09/548,942

Filed: April 13, 2000

For: METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES

Confirmation No.: 6934

Examiner: B. Lee

Group Art Unit: 2817

Attorney Docket No.: 2269-4161US
98-1265.00/US

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

July 26, 2004
Date

Signature

Leah J. Barrow
Name (Type/Print)

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following amendments and remarks are filed in response to the Examiner's remarks in the Office Action mailed April 26, 2004, the three-month shortened statutory period for response to which expires on July 26, 2004.

Amendments to the Specification begin on page 3 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Amendments to the Drawings begin on page 11 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Remarks/Arguments begin on page 12 of this paper.

Appendices A, B, and C, which include an amended specification and modified drawing figures are attached following page 31 of this paper.

IN THE SPECIFICATION:

Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date) please enter the substitute specification in clean form and including paragraph numbers **[0001]** through **[0037]** and Abstract attached hereto as Appendix A. A marked-up substitute specification to clearly identify amendments to the specification as required by 37 C.F.R. §§ 1.121(b)(3)(iii) is attached hereto as Appendix B. It is respectfully submitted that the substitute specification does not introduce new matter into the above-referenced patent application.

IN THE CLAIMS:

Claims 1-3, 6, 8-13, 15 and 19-22 have been amended herein. Claim 23 has been added as a new claim. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A printed circuit board, comprising:

a substrate having at least one electrically insulative layer; and

a plurality of conductive trace layers formed on opposing sides of the at least one electrically insulative layer, wherein at least one of the plurality of conductive trace layers includes a plurality of conductive traces including at least two signal traces and at least one voltage reference trace, the plurality of conductive traces being configured such that the at least one voltage reference trace is between the at least two signal traces, the at least one voltage reference trace also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

2. (Currently amended) The printed circuit board of claim 1, wherein at least one of the plurality of conductive traces includes at least one direction change in the length thereof over the at least one electrically insulative layer.

3. (Currently amended) The printed circuit board of claim 1, wherein the at least one electrically insulative layer comprises a plurality of insulative layers, each insulative layer separated by at least one conductive trace layer.

4. (Original) The printed circuit board of claim 1, wherein at least one of the conductive trace layers is a voltage reference plane.

5. (Original) The printed circuit board of claim 4, wherein the at least one voltage reference trace is coupled to the voltage reference plane.

6. (Currently amended) The printed circuit board of claim 1, further comprising a passivation layer deposited on at least one of the plurality of conductive trace layers.

7. (Previously presented) The printed circuit board of claim 1, wherein the at least one electrically insulative layer comprises two electrically insulative layers separated by a conductive layer, and wherein the at least one voltage reference trace is electrically coupled to the conductive layer.

8. (Currently amended) The printed circuit board of claim 1, wherein the at least one voltage reference trace is electrically coupled to at least one voltage reference bus.

9. (Currently amended) The printed circuit board of claim 1, wherein at least a portion of the plurality of conductive traces are embodied as vias.

10. (Currently amended) A printed circuit board, comprising at least one electrically insulative layer and at least one electrically conductive layer, the at least one electrically conductive layer comprising a voltage reference portion and at least one signal trace electrically isolated from the voltage reference portion, wherein the voltage reference portion has a greater surface area than the at least one signal trace, and wherein the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

11. (Currently amended) The printed circuit board of claim 10, wherein a majority of the at least one electrically conductive layer is comprised of the voltage reference portion.

12. (Currently amended) The printed circuit board of claim 10, wherein the voltage reference portion comprises a voltage reference bus with at least one voltage reference trace extending from the voltage reference bus.

13. (Currently amended) An electronic device, comprising:

at least one electrically insulative layer; and

at least one conductive layer, the at least one conductive layer comprising a voltage reference bus having at least one voltage reference trace extending therefrom and at least two signal traces electrically isolated from the at least one voltage reference trace, wherein the at least one voltage reference trace and the at least two signal traces are configured such that each signal trace is separated from each other signal trace by the at least one voltage reference trace, and wherein the at least one voltage reference trace is spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

14. (Previously presented) The electronic device of claim 13, further comprising a passivation layer deposited on the at least one conductive layer.

15. (Currently amended) A printed circuit board, comprising:

at least one voltage reference plane substantially coextensive with a portion of a substrate; and

at least one signal trace substantially coplanar with the at least one voltage reference plane and electrically isolated therefrom, the at least one voltage reference plane having a substantially greater surface area than the at least one signal trace, and wherein the

voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

16. (Original) The printed circuit board of claim 15, wherein the at least one signal trace is electrically isolated from the at least one voltage reference plane by at least one trough.

17. (Previously presented) The printed circuit board of claim 15, further comprising a passivation layer deposited on the at least one signal trace and the at least one voltage reference plane.

18. (Original) The printed circuit board of claim 15, wherein the at least one voltage reference plane is a substantially continuous voltage reference plane.

19. (Currently amended) A printed circuit board, comprising at least one voltage reference plane having at least one coplanar signal trace isolated therefrom, wherein the at least one voltage reference plane includes a surface area greater than any one signal trace, and wherein the voltage reference plane comprises a voltage reference bus having at least one voltage reference trace extending therefrom.

20. (Currently amended) An electronic system, comprising:

a processor;

a memory device;

at least one input device;

at least one output device; and

at least one data storage device;

wherein at least one of the processor, the memory device, the at least one input device, the at least one output device and the at least one data storage device includes a printed circuit board comprising:

a substrate having at least one electrically insulative layer; and

a plurality of conductive trace layers formed on opposing sides of the at least one electrically insulative layer, wherein each of the plurality of conductive trace layers includes a plurality of conductive traces including at least two signal traces and at least one voltage reference trace, the plurality of conductive traces being configured such that the at least one voltage reference trace is between the at least two signal traces, the at least one voltage reference trace also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

21. (Currently amended) The electronic system of claim 20, wherein at least one of the at least two signal traces includes at least one non-linear path over the at least one electrically insulative layer.

22. (Currently amended) An electronic system, comprising:

a processor;

a memory device;

at least one input device;

at least one output device; and

at least one data storage device;

wherein at least one of the processor, the memory device, the at least one input device, the at least one output device and the at least one data storage device includes a printed circuit board comprising:

at least one voltage reference plane substantially coextensive with a portion of a substrate; and

at least one signal trace substantially coplanar with the at least one voltage reference plane and electrically isolated therefrom, the at least one voltage reference plane having a substantially greater surface area than the at least one signal trace, and wherein the voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace..

23. (New) An electronic system, comprising:

a processor;

a memory device;

at least one input device;

at least one output device;

at least one data storage device; and

a printed circuit board comprising:

a substrate having at least one electrically insulative layer; and

a plurality of conductive trace layers formed on opposing sides of the at least one electrically insulative layer, wherein each of the plurality of conductive trace layers includes a plurality of conductive traces including at least two signal traces and at least one voltage reference trace, the plurality of conductive traces being configured such that the at least one voltage reference trace is between the at least two signal traces, the at least one voltage reference trace also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

IN THE DRAWINGS:

Formal drawings annotated in red with proposed changes to address the Examiner's concerns are attached hereto as Appendix C. Proposed changes appear in FIGS. 2, 8, 12, and 13.

REMARKS/ARGUMENTS

The Office Action mailed April 26, 2004, has been received and reviewed. Claims 1 through 23 are currently pending in the application. Claims 1 through 22 stand rejected. Claim 23 has been added as a new claim. Applicant has amended claims 1-3, 6, 8-13, 15 and 19-22, and respectfully requests reconsideration of the application as amended herein.

A substitute specification has been submitted and is herewith attached. The substitute specification includes minor modifications described below, as requested by the Examiner. In addition to the modifications described below, the substitute specification includes paragraph numbering and changes pursuant to the previously submitted preliminary amendment of June 29, 2000.

In the specification, paragraph [0003] has been amended to clarify the description. The date parenthetical of the Ishii patent has been modified. "Sep" has been replaced with "issued September."

In the specification, paragraph [0004] has been amended to clarify the description. The date parenthetical of the Gagnon patent has been modified. "Jul" has been replaced with "issued July."

In the specification, paragraph [0006] has been amended to clarify the description. The date parenthetical of the Yamamoto patent has been modified. "Sep" has been replaced with "issued September." The date parenthetical of the Kametani patent has been modified. "Dec" has been replaced with "issued December." The date parenthetical of the Yamamoto patent has been modified. "Dec" has been replaced with "issued December." The date parenthetical of the Millar patent has been modified. "Aug" has been replaced with "issued August."

In the specification, the title "Brief Description of the Several Views of the Drawings" has been replaced with "Brief Description of the Drawings."

In the specification, paragraph [0028] has been amended to clarify the description of Figure 4. The phrase "between the upper surface of the substrate 12 and the upper surface of the

circuit trace 14," has been inserted after the phrase "and the height ("H")" to both clarify the term "H" and define substrate 12 as shown in Figure 4.

In the specification, paragraph [0031] has been amended to clarify the description of Figure 8. On the first line of the paragraph, the term "substrates" has been replaced with the term "substrate," because Figure 8 only depicts one substrate. The term "adjacent" has been inserted into the third line of the paragraph to clarify the phrase that now reads "placed between two adjacent signal traces." The reference numeral "21" has been added on the sixth line of the paragraph after the term "second surface" to conform with the labeling of Figure 8.

In the specification, paragraph [0034] has been amended to clarify the description of Figure 13. On line four of the paragraph, after the term "gap 40," the parenthetical "(see Figure 13)" has been inserted to properly reference the reference numeral "40." Also, on the twentieth line of the paragraph, after the term "passivation layer," the reference numeral "50" has been inserted, followed by the phrase "(see Figures 8, 12 and 13)," in order to adequately explain the corresponding modifications to the figures.

In the specification, paragraph [0035] has been amended to clarify the description of Figure 14. The acronym "("PCB")" has been inserted after the term "printed circuit board," on the second line of the paragraph. Accordingly, on the fifteenth line of the paragraph, the term "printed circuit board" has been replaced with "PCB." Also, on the seventeenth line, the term "respective" has been added before the term "cache" for clarification purposes.

In amended Figure 2, the reference numerals "4" and "6" have been removed in order to eliminate redundancy with previously used reference numerals.

In amended Figure 8, as requested by the Examiner, a passivation layer as described in paragraph [0034] of the specification has been added and labeled with reference numeral "50."

In amended Figure 12, as requested by the Examiner, a passivation layer as described in paragraph [0034] of the specification has been added and labeled with reference numeral "50."

In amended Figure 13, as requested by the Examiner, a passivation layer as described in paragraph [0034] of the specification has been added and labeled with reference numeral "50."

35 U.S.C. § 112 Claim Rejections

Claims 2, 3, 6, 8, 9, 11, 12, 20, 21, and 22 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

In reference to claim 2, the examiner notes that it is unclear how the element "at least one trace" relates to independent claim 1. As a remedy, both claims 1 and 2 have been amended. Claim 1 originally included the elements "at least two signal traces" and "at least one voltage reference trace," but thereafter referred only to "the traces." To clarify claim 1, and in accordance with the language in the specification, the element of a "plurality of conductive traces" has been inserted to collectively refer to both "at least two signal traces" and "at least one voltage reference trace." In claim 2, corresponding language has been included. The old language of "at least one trace" has been replaced with "at least one of the plurality of conductive traces," in reference to independent claim 1.

Also in reference to claim 2, the examiner notes that the language "its length" is unclear. The examiner suggests replacing "its length" with "the length thereof." Accordingly, this change has been made.

In reference to claim 3, the examiner notes that the phrase "insulative layer" should follow "each." Accordingly, claim 3 now includes the phrase "each insulative layer."

In reference to claim 6, the examiner notes that it is unclear how the element "at least one of the conductive trace layers" relates to claim 1. As a remedy, both claims 1 and 2 have been amended. Claim 1 originally referred to "at least two conductive trace layers," and then later to "at least one of the at least two conductive trace layers." To clarify this language, and without changing the substance or scope of the claim, the element of "at least two conductive trace layers" has been replaced with a "plurality of conductive trace layers." The later reference in claim 1 follows as "at least one of the plurality of conductive trace layers." Accordingly, claim 6 has been modified to refer to "at least one of the plurality of conductive trace layers."

In reference to claim 8, the examiner notes that it is unclear how the element "at least one of the at least two conductive trace layers" relates to claim 1. In order to clarify this recitation, and to simplify the language of the entire claim, much of the language of claim 8 has been removed. The phrase "wherein at least one of the at least two conductive trace layers further comprises at least one voltage reference bus" has been removed. Accordingly, the identifier "the" after the phrase "is electrically coupled to" has been removed. These changes do not alter the scope or substance of claim 8, but merely simplify the language of claim 8.

In reference to claim 9, the examiner notes that it is unclear how the element "traces" is intended to be recited. The element "traces" of claim 9 refers collectively to the "at least two signal traces" and the "at least one voltage reference trace" of claim 1. As previously asserted herein, the language of claim 1 has been modified to include the element a "plurality of conductive traces," referring collectively to the "at least two signal traces" and the "at least one voltage reference trace." Accordingly, in claim 9, "the traces" has been modified to instead read "the plurality of conductive traces."

In reference to claim 11, the examiner notes that it is unclear whether the "at least one electrically conductive layer" may be properly characterized as being "comprised *in* the voltage reference portion" (Emphasis added). To clarify, the phrase "comprised in" has been replaced with the phrase "comprised of."

In reference to claim 12, the examiner notes that it is unclear whether "the voltage reference bus" and "traces extending therefrom" may properly depend from claim 10, which states that the voltage reference portion has "a greater surface area than the at least one signal trace." Claim 12 further defines and narrows the "voltage reference portion" of claim 10. Accordingly, the language of claim 12 has been modified to more clearly show the relationship between the elements of claim 12 and the "voltage reference portion" element of claim 10. In claim 13, the phrase "having" has been replaced with the phrase "with at least one." Additionally, the word "therefrom" was replaced with the more descriptive "from the voltage reference bus." Thus, the "voltage reference portion" of claim10 is further narrowed by claim 12 to comprise of

"a voltage reference bus with at least one voltage reference trace extending from the voltage reference bus."

In reference to claim 20, the examiner again notes that the element "traces" is unclear. The element "traces" was intended to refer collectively to the "at least two signal traces" and the "at least one voltage reference trace." To clarify this language, claim 20 has been modified to include the phrase "a plurality of conductive traces including" inserted just before the element "at least two signal traces." Thus, the element "a plurality of conductive traces" includes both the elements of "at least two signal traces" and "at least one voltage reference trace." Accordingly, the phrase "traces" has been modified to instead read "the plurality of conductive traces." Additionally, a "the" has been added after the phrase "such that," and "the at least" replaces the phrase "each of the," thus maintaining a proper antecedent basis.

Also in reference to claim 20, the examiner notes that it is unclear what characterizes "at least one component of the electronic system." The "at least one component" was intended to refer to at least one of the other elements of the electrical system outlined in claim 20. Accordingly, the phrase "at least one component of the electronic system" has been replaced with "at least one of the processor, the memory device, the at least one of an input device, the at least one of an output device, and the at least one of a data storage device."

In reference to claim 21, the examiner notes that the phrase "in its extent" is unnecessary and should be deleted. Accordingly, the phrase has been deleted from claim 21.

In reference to claim 22, the examiner notes that it is unclear what characterizes "at least one component of the electronic system." The components of the electrical system include those elements previously specified in the claim. To clarify this, the phrase "at least one component of the electronic system" has been replaced with "at least one of the processor, the memory device, the at least one of an input device, the at least one of an output device and the at least one of a data storage device."

35 U.S.C. § 102 Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,040,524 to Kobayashi et al.

Claims 1 through 5, 7, 9, 10, 11, 15, 16, 18, and 19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kobayashi et al. (U.S. Patent No. 6,040,524). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Kobayashi describes a printed circuit board comprising a dielectric lamina with two opposing surfaces (Col. 6, lines 42-49). On one of the surfaces is deposited a layer of microstrips constituting signal lines and ground areas, the ground areas arranged between the signal lines (Col. 6, lines 49-51, 61-63). On the other surface is a ground plane (Col 6, lines 54-55). Conductive means connect the ground plane to the ground areas interleaved with the signal lines (Col 7, lines 2-5). Implementation of the described printed circuit board arrangement onto multiple layer printed circuit boards is also taught (Col. 7, lines 26-63).

However, Kobayashi does not teach the spatial periodic coupling of a ground area or a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the ground area or voltage reference trace. As described in ¶ [0030] of the specification of the above-referenced application, periodic coupling of a reference trace is necessary to maintain a consistent voltage on the reference trace. In the absence of sufficient periodic coupling, the reference trace instead acts as an antenna. Thus, not only must the coupling to a reference voltage be periodic, the periodicity must also result in sufficiently dense coupling to avoid drifting of the reference trace voltage. The necessary density may be determined prior to the final manufacturing of the printed circuit board.

Because Kobayashi does not teach the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-

referenced application, claim 1 has been amended by requiring that "the at least one voltage reference trace [be] also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Therefore, it is respectfully submitted that Kobayashi does not anticipate each and every element of independent amended claim 1. Thus, under 35 U.S.C. § 102(e), independent amended claim 1 is allowable over Kobayashi.

Claims 2-5, 7 and 9 are each allowable, among other reasons, as depending either directly or indirectly from amended claim 1, which is allowable.

Independent claim 10 is directed to a printed circuit board comprising at least one electrically conductive layer which further includes a voltage reference portion and at least one signal trace. The voltage reference portion has a greater surface area than the at least one signal trace.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Kobayashi neither expressly nor inherently describes a printed circuit board that includes a voltage reference portion with at least one voltage reference trace spatially periodically coupled to a reference voltage. Accordingly, claim 10 has been amended to require that "the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Kobayashi does not anticipate each and every element of independent amended claim 10. Thus, under 35 U.S.C. § 102(e), independent amended claim 10 is allowable over Kobayashi.

Claim 11 is allowable, among other reasons, as depending either directly or indirectly from amended claim 10, which is allowable.

Independent claim 15 is directed to a printed circuit board that comprises at least one voltage reference plane substantially coextensive with a portion of a substrate.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Kobayashi neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage. Accordingly, claim 15 has been amended to include "the voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Kobayashi does not anticipate each and every element of independent amended claim 15. Thus, under 35 U.S.C. § 102(e), independent amended claim 15 is allowable over Kobayashi.

Claims 16 and 18 are allowable, among other reasons, as depending either directly or indirectly from amended claim 15, which is allowable.

Independent claim 19 is directed to a printed circuit board that comprises at least one voltage reference plane and a coplanar signal trace isolated therefrom.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Kobayashi neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage. Accordingly, claim 19 has been amended to include "the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Kobayashi does not anticipate each and every element of independent amended claim 19. Thus, under 35 U.S.C. § 102(e), independent amended claim 19 is allowable over Kobayashi.

Anticipation Rejection Based on German Patent No. DD 239 899 A1

Claims 1, 3 through 5, 15, 16, 18, and 19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by German Patent No. DD 239 899 A1 (hereinafter "the East German Patent"). Applicant respectfully traverses this rejection, as hereinafter set forth.

The East German reference describes a double-sided circuit board whereon pairs of signal lines and ground lines may be formed on either side of an insulating substrate. The widths of the ground lines are twice the widths of the corresponding signal lines. Ground lines are depicted in the accompanying figures as interleaved with the signal lines.

However, like Kobayashi, the East German patent does not teach the spatial periodic coupling of a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the extent of the voltage reference trace.

Because the East German patent does not teach the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-referenced application, claim 1 has been amended to include "the at least one voltage reference trace [be] also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Therefore, it is respectfully submitted that the East German patent does not anticipate each and every element of independent amended claim 1. Thus, under 35 U.S.C. § 102(b), independent amended claim 1 is allowable over the East German patent.

Claims 3, 4 and 5 are each allowable, among other reasons, as depending either directly or indirectly from amended claim 1, which is allowable.

Claim 5 is additionally allowable because the East German patent lacks any express or inherent description that the printed circuit board includes at least one voltage reference trace coupled to a voltage reference plane. Although Figure 4 of the East German patent depicts a voltage reference plane on one conductive layer of the substrate, it doesn't appear to Applicant that the voltage reference plane is coupled to the plurality of ground lines depicted on other

conductive layers. It is possible that the voltage reference plane holds a reference voltage other than that shared by the ground lines. Hence, it is not clear that the assumption that the depicted voltage reference plane and the ground lines are inherently coupled is a valid assumption.

Independent claim 15 is directed to a printed circuit board that comprises at least one voltage reference plane substantially coextensive with a portion of a substrate.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that the East German patent neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage. Accordingly, claim 15 has been amended to include "the voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, the East German patent does not anticipate each and every element of independent amended claim 15. Thus, under 35 U.S.C. § 102(b), independent amended claim 15 is allowable over the East German patent.

Claims 16 and 18 are allowable, among other reasons, as depending either directly or indirectly from amended claim 15, which is allowable.

Independent claim 19 is directed to a printed circuit board that comprises at least one voltage reference plane and a coplanar signal trace isolated therefrom.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that the East German patent neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage. Accordingly, claim 19 has been amended to include "the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, the East German patent does not

anticipate each and every element of independent amended claim 19. Thus, under 35 U.S.C. § 102(b), independent amended claim 19 is allowable over the East German patent.

Anticipation Rejection Based on U.S. Patent No. 3,398,232 to Hoffman

Claims 1, 8, 9, and 13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hoffman (U.S. Patent No. 3,398,232). Applicant respectfully traverses this rejection, as hereinafter set forth.

Hoffman describes a printed circuit board comprising a plurality of signal and reference traces interweaved together on at least two sides of a substrate. Col. 3, lines 17-35; Col. 4, lines 4-18. The reference traces are connected to a common reference bus. Col. 6, lines 16-24. Conducting plugs or vias connect signal traces or reference traces on opposing sides of the printed circuit board. Col. 4, lines 24-37.

However, Hoffman does not teach the spatial periodic coupling of a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the extent of the voltage reference trace. Consequently, because Hoffman does not teach the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-referenced application, claim 1 has been amended to include "the at least one voltage reference trace [be] also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Therefore, it is respectfully submitted that Hoffman does not anticipate each and every element of independent amended claim 1. Thus, under 35 U.S.C. § 102(b), independent amended claim 1 is allowable over Hoffman.

Claims 8 and 9 are each allowable, among other reasons, as depending either directly or indirectly from amended claim 1, which is allowable.

Independent claim 13 is directed to an electronic device that includes at least one voltage reference trace and at least two signal traces.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Hoffman neither expressly nor inherently describes an electronic device that includes a voltage reference trace spatially periodically coupled to a reference voltage. Accordingly, claim 13 has been amended to require that "the at least one voltage reference trace [is] spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Hoffman does not anticipate each and every element of independent amended claim 13. Thus, under 35 U.S.C. § 102(b), independent amended claim 13 is allowable over Hoffman.

Anticipation Rejection Based on U.S. Patent No. 4,130,723 to Wakeling

Claims 1, 2, 10, 11, 15, 16, and 19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wakeling (U.S. Patent No. 4,130,723). Applicant respectfully traverses this rejection, as hereinafter set forth.

Wakeling describes a printed circuit board comprising a double-sided insulated substrate with conductive trace layers on either or both sides. Col. 4, lines 15-32. Alternating signal tracks and ground tracks may be deposited on either side of the substrate. Col. 2, lines 9-11. Ground tracks further connect with a periphery track. Col. 2, lines 24-25. The ground tracks are wider than the signal tracks, and may comprise a majority of a conductive layer.

However, Wakeling does not teach the spatial periodic coupling of a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the extent of the voltage reference trace. Consequently, because Wakeling does not teach the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-referenced application, claim 1 has been amended to include "the at least one voltage reference trace [be] also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a

substantially consistent reference voltage throughout the at least one voltage reference trace." Therefore, it is respectfully submitted that Wakeling does not anticipate each and every element of independent amended claim 1. Thus, under 5 U.S.C. § 102(b), independent amended claim 1 is allowable over Wakeling.

Claim 2 is allowable, among other reasons, as depending either directly or indirectly from amended claim 1, which is allowable.

Independent claim 10 is directed to a printed circuit board comprising at least one electrically conductive layer which further includes a voltage reference portion and at least one signal trace. The voltage reference portion has a greater surface area than the at least one signal trace.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Wakeling neither expressly nor inherently describes a printed circuit board that includes a voltage reference portion spatially periodically coupled to a reference voltage. Accordingly, claim 10 has been amended to include "the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Wakeling does not anticipate each and every element of independent amended claim 10. Thus, under 35 U.S.C. § 102(b), independent amended claim 10 is allowable over Wakeling.

Claim 11 is allowable, among other reasons, as depending either directly or indirectly from amended claim 10, which is allowable.

Independent claim 15 is directed to a printed circuit board that comprises at least one voltage reference plane substantially coextensive with a portion of a substrate.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Wakeling neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage.

Accordingly, claim 15 has been amended to include "the voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Wakeling does not anticipate each and every element of independent amended claim 15. Thus, under 35 U.S.C. § 102(b), independent amended claim 15 is allowable over Wakeling.

Claim 16 is allowable, among other reasons, as depending either directly or indirectly from amended claim 15, which is allowable.

Independent claim 19 is directed to a printed circuit board that comprises at least one voltage reference plane and a coplanar signal trace isolated therefrom.

For the same reasons provided above with respect to independent claim 1, it is respectfully submitted that Wakeling neither expressly nor inherently describes a printed circuit board that includes a voltage reference plane spatially periodically coupled to a reference voltage. Accordingly, claim 19 has been amended to include "the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Hence, Wakeling does not anticipate each and every element of independent amended claim 19. Thus, under 35 U.S.C. § 102(b), independent amended claim 19 is allowable over Wakeling.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. §§ 102(b) and 102(e) rejections of claims 1-5, 7-11, 13, 15, 16, 18 and 19 be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Claims 6, 14, 17, 20, 21 and 22 stand rejected under 35 U.S.C. § 103.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Obviousness Rejection Based on U.S. Patent No. 6,040,524 to Kobayashi et al or U.S. Patent No. 4,130,723 to Wakeling, in View of U.S. Patent No. 6,373,740 to Forbes et al.

Claims 6 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi et al. (U.S. Patent No. 6,040,524) or Wakeling (U.S. Patent No. 4,130,723), in view of Forbes et al. (U.S. Patent No. 6,373,740). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claim 6 is allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable. Claim 17 is allowable, among other reasons, as depending either directly or indirectly from claim 15, which is allowable.

Moreover, it is respectfully submitted that claims 6 and 17 are both allowable since the asserted combinations of Forbes with one of Kobayashi or Wakeling do not support a *prima facie* case of obviousness against either of these claims under 35 U.S.C. § 103(a).

In particular, one of ordinary skill in the art would not have been motivated to combine the teachings of Forbes with the teachings of either Kobayashi or Wakeling.

This is because Forbes does not provide one of ordinary skill in the art with any motivation to use a passivation layer whereon no further conductive layers will be deposited. Forbes teaches the use of an insulating layer on top of a conductive layer to facilitate deposition of an additional conductive layer. Col. 3, line 46 to Col. 4, line 31. As is well known in the art of printed circuit board design, vertical stacking of conductive traces is not possible without a

means for insulating each conductive trace layer from another. Deposition of an insulating layer between conductive layers is one such means. Application of insulation deposition means may be obvious to one skilled in the art *when an additional conductive layer is to be vertically stacked on top of existing conductive layers*. However, in the above-referenced application, additional vertical stacking is not anticipated, and hence, it would not be obvious to one skilled in the art to combine the teachings of Forbes with those of either Kobayashi or Wakeling.

As there is no motivational link between Forbes and either Kobayashi or Wakeling, it is respectfully submitted that any motivation to combine the teachings of Forbes with those of either Kobayashi or Wakeling could only have been improperly gleaned from the hindsight provided by the disclosure of the above-referenced application.

For these reasons, it is respectfully submitted that under 35 U.S.C. § 103(a), claims 6 and 17 are both allowable over the combination of Forbes with any of Kobayashi and Wakeling.

Obviousness Rejection Based on U.S. Patent No. 3,398,232 to Hoffman in View of U.S. Patent No. 6,373,740 to Forbes et al.

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hoffman (U.S. Patent No. 3,398,232) in view of Forbes et al. (U.S. Patent No. 6,373,740). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claim 14 is allowable, among other reasons, as depending either directly or indirectly from claim 13, which is allowable.

Moreover, it is respectfully submitted that claim 14 is allowable since the asserted combination of Forbes with Hoffman does not support a *prima facie* case of obviousness against this claim under 35 U.S.C. § 103(a).

In particular, one of ordinary skill in the art would not have been motivated to combine the teachings of Forbes with the teachings of Hoffman.

For the same reason provided above with respect to claims 6 and 17, one of ordinary skill in the art would not have been motivated to combine the teachings of Forbes with Hoffman in the manner that has been asserted. In particular, there would have been no motivation for one of

ordinary skill in the art, before the earliest priority date for the above-referenced application, to have used a passivation layer whereon no further conductive layers will be deposited. In the above-referenced application, additional vertical stacking is not anticipated, and hence, it would not be obvious to one skilled in the art to combine the teachings of Forbes with those of Hoffman.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 103(a), claim 14 is allowable over the combination of Forbes with Hoffman.

Obviousness Rejection Based on U.S. Patent No. 6,373,740 to Forbes et al. in View of U.S. Patent No. 6,040,524 to Kobayashi et al or U.S. Patent No. 4,130,723 to Wakeling

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Forbes et al. (U.S. Patent No. 6,373,740) in view of Kobayashi et al. (U.S. Patent No. 6,040,524) or Wakeling (U.S. Patent No. 4,130,723). Applicant respectfully traverses this rejection, as hereinafter set forth.

It is respectfully submitted that claim 20 is allowable since the asserted combinations of one of Kobayashi or Wakeling with Forbes does not support a *prima facie* case of obviousness against either of these claims under 35 U.S.C. § 103(a).

In particular, combining one of Kobayashi or Wakeling with Forbes does not teach or suggest all of the claim limitations of claim 20.

Neither Kobayashi nor Wakeling teach the spatial periodic coupling of a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the extent of the voltage reference trace. As described in the specification of the above-referenced application, periodic coupling of a reference trace is necessary to maintain a consistent voltage on the reference trace. In the absence of sufficient periodic coupling, the reference trace instead acts as an antenna. Thus, not only must the coupling to a reference voltage be periodic, the periodicity must also result in sufficiently dense coupling to avoid drifting of the reference trace voltage. The necessary density may be determined prior to the final manufacturing of the printed circuit board.

Because neither Kobayashi nor Wakeling teaches the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-referenced application, claim 20 has been amended to require that "the at least one voltage reference trace [be] also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace." Therefore, it is respectfully submitted that combining one of either Kobayashi or Wakeling with Forbes does not teach or suggest all of the claim limitations of claim 20. Thus, under 5 U.S.C. § 103(a), independent claim 20 is allowable over the combination of one of Kobayashi or Wakeling with Forbes.

Obviousness Rejection Based on U.S. Patent No. 6,373,740 to Forbes et al. in View of Either U.S. Patent No. 6,040,524 to Kobayashi et al or U.S. Patent No. 4,130,723 to Wakeling

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Forbes et al. (U.S. Patent No. 6,373,740) in view of either Kobayashi et al. (U.S. Patent No. 6,040,524) or Wakeling (U.S. Patent No. 4,130,723). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claim 21 is allowable, among other reasons, as depending either directly or indirectly from claim 20, which is allowable.

Moreover, it is respectfully submitted that claim 21 is allowable since the asserted combination of one of Kobayashi or Wakeling with Forbes does not support a *prima facie* case of obviousness against this claim under 35 U.S.C. § 103(a).

In particular, combining one of Kobayashi or Wakeling with Forbes does not teach or suggest all of the claim limitations of claim 21.

For the same reason provided above with respect to claim 20, combining one of Kobayashi or Wakeling with Forbes does not teach or suggest the additional claim limitation added to claim 20. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 103(a), claim 21 is allowable over the combination of one of Kobayashi or Wakeling with Forbes.

Obviousness Rejection Based on U.S. Patent No. 6,373,740 to Forbes et al. in View of Either U.S. Patent No. 4,130,723 to Wakeling or German Patent No. DD 239 899 A1

Claim 22 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Forbes et al. (U.S. Patent No. 6,373,740) in view of either Wakeling (U.S. Patent No. 4,130,723) or German Patent No. DD 239 899 A1. Applicant respectfully traverses this rejection, as hereinafter set forth.

It is respectfully submitted that claim 22 is allowable since the asserted combinations of one of Wakeling or the East German patent with Forbes does not support a *prima facie* case of obviousness against either of these claims under 35 U.S.C. § 103(a).

In particular, combining one of Wakeling or the East German patent with Forbes does not teach or suggest all of the claim limitations of claim 22.

Neither Wakeling nor the East German patent teach the spatial periodic coupling of a voltage reference trace to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the extent of the voltage reference trace.

Because neither Wakeling nor the East German patent teaches the sufficiently periodic coupling of a voltage reference trace to a reference voltage, and because this is taught in the specification of the above-referenced application, claim 22 has been amended by the additional phrase "and wherein the voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace. Therefore, it is respectfully submitted that combining one of either Wakeling or the East German patent with Forbes does not teach or suggest all of the claim limitations of claim 22. Thus, under 5 U.S.C. § 103(a), independent claim 22 is allowable over the combination of one of Wakeling or the East German patent with Forbes.

For the foregoing reasons, withdrawal of the 35 U.S.C. § 103(a) rejections of claims 6, 14, 17 and 20-22 is respectfully requested.

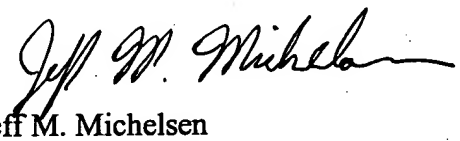
ENTRY OF AMENDMENTS

The amendments to claims 1-3, 6, 8-13, 15 and 19-22 above should be entered by the Examiner. New claim 23 should also be entered by the Examiner. The Examiner should enter these amendments and new claim because the amendments and new claim are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1-23 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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Date: July 26, 2004
JMM/nj:rh
Document in ProLaw

APPENDIX C
Proposed Drawing Corrections

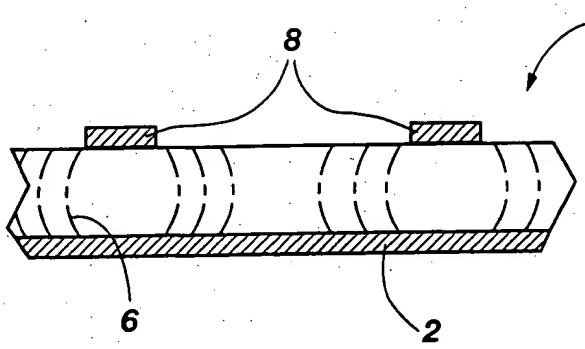

Fig. 1
(PRIOR ART)

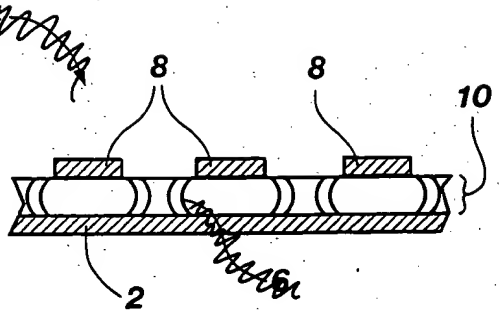

Fig. 2
(PRIOR ART)

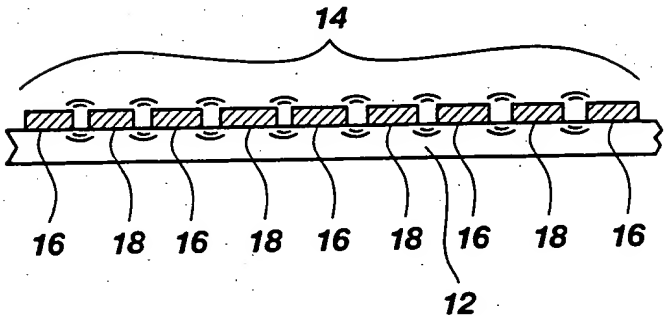

Fig. 3

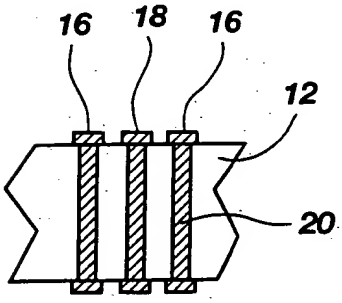

Fig. 5

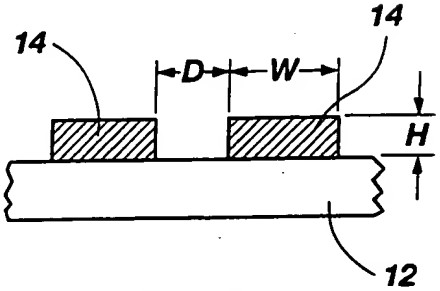

Fig. 4

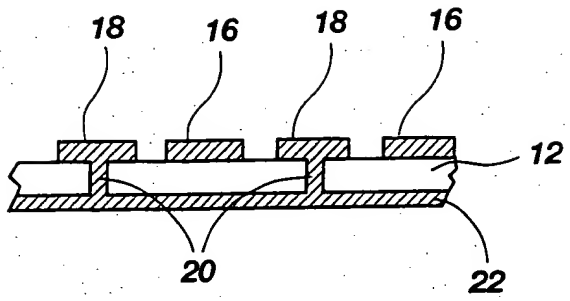

Fig. 6

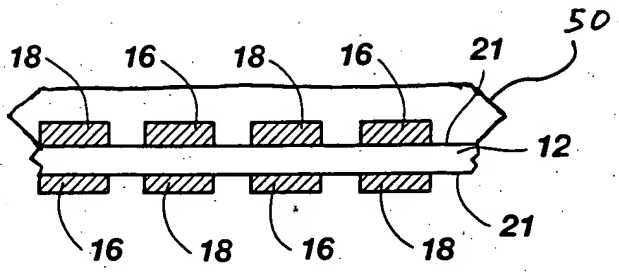

Fig. 8

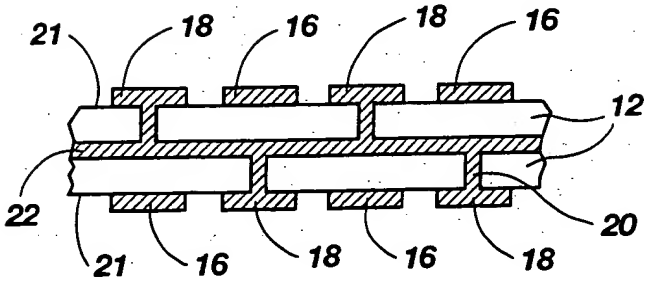

Fig. 7

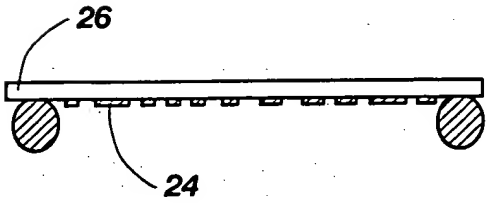

Fig. 11

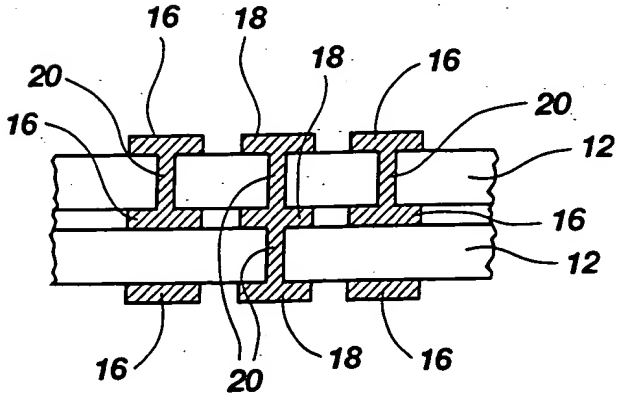

Fig. 10

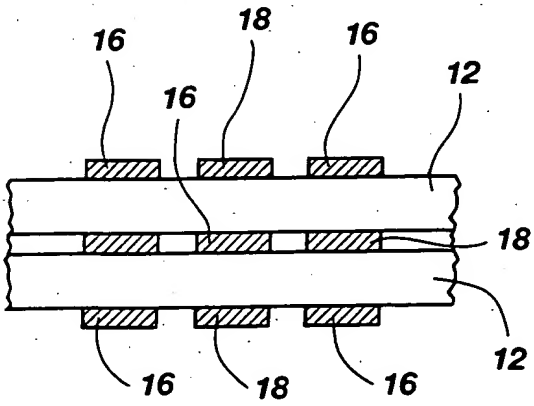

Fig. 9

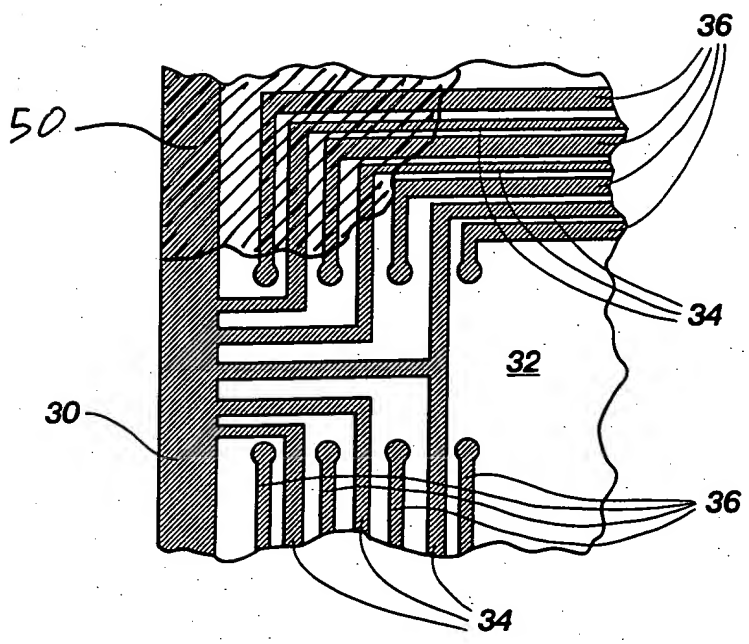

Fig. 12

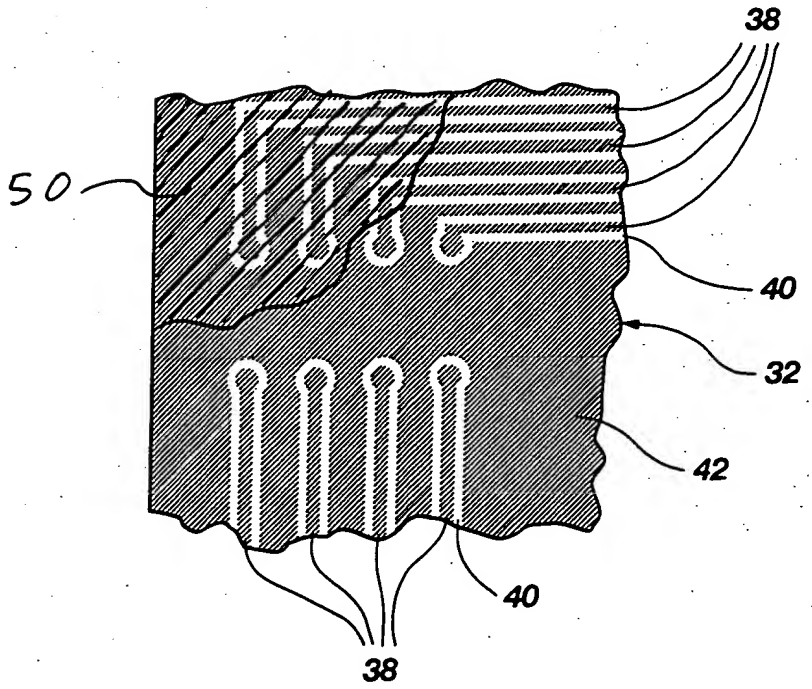

Fig. 13

THE PATENT & TRADEMARK OFFICE MAILROOM DATE STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Transmittal Form (1 page in duplicate); Amendment in response to office action dated January 4, 2006 (16 pages); Appendix including Replacement Sheet (1 sheet); Annotated Sheet Showing Changes (1 sheet)

Invention:	METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES
Applicant(s):	Warren M. Farnworth
Filing Date:	April 13, 2000
Serial No.:	09/548,942
Date Sent:	April 4, 2006 via first class mail
Docket No.:	2269-4161US
JMM/eg	

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TRASKBRITT, P.C.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Warren M. Farnworth

Serial No.: 09/548,942

Filed: April 13, 2000

For: METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES

Confirmation No.: 6934

Examiner: B. Lee

Group Art Unit: 2817

Attorney Docket No.: 2269-4161US
(98-1265.00/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

April 4, 2006
Date

Signature

Erika Gandre
Name (Type/Print)

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following amendments and remarks are filed in response to the Examiner's remarks in the Office Action mailed January 4, 2006, the three-month shortened statutory period for response to which expires on April 4, 2006.

Amendments to the Specification begin on page 3 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Amendments to the Drawings begin on page 8 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Remarks/Arguments begin on page 9 of this paper.

An **Appendix** including amended drawing figures is attached following page 16 of this paper.

IN THE SPECIFICATION:

Please replace paragraph 0032 with the following.

[0032] Figure 11 illustrates an embodiment of the present invention wherein circuit traces 24 are placed on the surface of a semiconductor substrate 26, more particularly, in a flip-chip ball grid array ("BGA") application. Like previous embodiments, the circuit traces 24 are configured such that a voltage reference trace 28 is placed between each of two signal traces 24 so that no signal trace 24 is placed immediately adjacent another signal trace 24. At least one of the solder balls 29 is operably coupled to at least one signal trace 24 and at least one solder ball 29 is operably coupled to a voltage reference trace 28.

IN THE CLAIMS:

None of the claims have been amended herein. All of the pending claims 24-26 and 28-31 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as previously amended.

Listing of Claims:

Claims 1-23. (Canceled)

24. (Previously Presented) An electronic device, comprising:

a semiconductor substrate;

an electrically conductive layer disposed on at least one side of the semiconductor substrate, comprising;

a voltage reference plane substantially covering the at least one side of the semiconductor substrate and configured for operable coupling to a voltage reference signal;

a plurality of signal trace slots disposed in the voltage reference plane; and

a plurality of signal traces disposed in the plurality of signal trace slots;

wherein the plurality of signal traces are electrically isolated from the voltage reference plane by a gap in the electrically conductive layer with a gap distance sufficient to avoid an electrical short between the plurality of signal traces and the voltage reference plane; and

wherein the voltage reference plane provides a continuous electrical connection around each of the plurality of signal trace slots such that at least a portion of the voltage reference plane is disposed between any two of the plurality of signal traces to reduce cross talk between signals carried by the any two of the plurality of signal traces; and

a plurality of solder balls disposed on the at least one side of the semiconductor substrate,

wherein at least one of the plurality of solder balls is operably coupled to at least one of

the plurality of signal traces and at least one of the plurality of solder balls is operably coupled to the voltage reference signal.

25. (Previously Presented) The electronic device of claim 24, further comprising a passivation layer disposed on the electrically conductive layer.

26. (Previously Presented) The electronic device of claim 24, wherein at least one of the plurality of signal traces includes at least one direction change in the length thereof over the semiconductor substrate.

Claim 27. (canceled)

28. (Previously Presented) The electronic device board of claim 24, wherein the semiconductor substrate includes:

an electrically insulative layer disposed on the electrically conductive layer; and

an additional electrically conductive layer disposed on the electrically insulative layer, comprising;

an additional voltage reference plane substantially covering the electrically insulative layer and configured for operable coupling to the voltage reference signal;

a plurality of additional signal trace slots disposed in the additional voltage reference plane; and

a plurality of additional signal traces disposed in the plurality of additional signal trace slots;

wherein the plurality of additional signal traces are electrically isolated from the additional voltage reference plane by an additional gap in the additional electrically conductive layer with an additional gap distance sufficient to avoid an electrical short between the plurality of additional signal traces and the additional voltage reference plane; and

wherein the additional voltage reference plane provides a continuous electrical connection around each of the plurality of additional signal trace slots such

that at least a portion of the additional voltage reference plane is disposed between any two of the plurality of additional signal traces to reduce cross talk between signals carried by the any two of the plurality of additional signal traces.

29. (Previously Presented) The electronic device of claim 28, wherein at least a portion of the plurality of signal traces are operably coupled to at least a portion of the plurality of additional signal traces by vias provided through the electrically insulative layer.

30. (Previously Presented) The electronic device of claim 28, wherein the voltage reference plane is operably coupled to the additional voltage reference plane by vias provided through the electrically insulative layer.

31. (Previously Presented) An electronic system, comprising:

a processor;

a memory device;

at least one input device;

at least one output device; and

at least one data storage device;

wherein at least one of the processor, the memory device, the at least one input device, the at least one output device and the at least one data storage device includes an electronic device comprising:

a semiconductor substrate; and

an electrically conductive layer disposed on at least one side of the semiconductor substrate, comprising;

a voltage reference plane substantially covering the at least one side of the semiconductor substrate and configured for operable coupling to a voltage reference signal;

a plurality of signal trace slots disposed in the voltage reference plane; and

a plurality of signal traces disposed in the plurality of signal trace slots;

wherein the plurality of signal traces are electrically isolated from the voltage reference plane by a gap in the electrically conductive layer with a gap distance sufficient to avoid an electrical short between the plurality of signal traces and the voltage reference plane; and

wherein the voltage reference plane provides a continuous electrical connection around each of the plurality of signal trace slots such that at least a portion of the voltage reference plane is disposed between any two of the plurality of signal traces to reduce cross talk between signals carried by the any two of the plurality of signal traces; and

a plurality of solder balls disposed on the at least one side of the semiconductor substrate, wherein at least one of the plurality of solder balls is operably coupled to at least one of the plurality of signal traces and at least one of the plurality of solder balls is operably coupled to the voltage reference signal.

IN THE DRAWINGS:

The attached sheet of drawings includes changes to FIG. 11. This sheet, which includes FIGS. 6-11, replaces the previous drawing sheet including FIGS. 6-11. In FIG. 11, the solder balls are shown as being connected to at least one signal and at least connected to the voltage reference signal, as suggested by the Examiner. (See attached Replacement Sheet and Annotated Sheet Showing Changes.)

REMARKS

The Office Action mailed January 4, 2006, has been received and reviewed. Claims 24 through 26, and 28 through 31, are currently pending in the application. Claims 24 through 26, and 28 through 31, stand rejected. Applicant respectfully requests reconsideration of the application with respect to the analysis presented herein.

Objections to Drawings

Fig. 11 has been modified to show the solder balls being connected to at least one signal and at least connected to the voltage reference signal, as suggested by the Examiner.

Objections to Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter.

The Examiner states that:

> "[t]he specification needs to provide an explicit description with respect to the FIG. 11 embodiment of the connection of the solder balls to at least one signal trace and the voltage reference signal as recited in amended claims 24 and 31. Since this amended limitation is considered not to be "new matter," then an amendment to the fig. 11 adding the amended claim limitation would be appropriate."

Appropriate amendments have been made to paragraph 0032 describing the connection to the solder balls.

35 U.S.C. § 112 Claim Rejections

Claims 24 through 26, 28 through 31, stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

The Examiner states that:

> "[i]t appears that the reference to the "semiconductor substrate" and "solder balls" relates to the embodiment depicted and describe relative to "figure 11", while the reference to the slotted voltage reference plane and isolated signal traces relate to the embodiment of "figure 13". However, there does not appear to be any disclosure in the original specification as to an embodiment combining the "semiconductor substrate/solder balls embodiment of "figure 11" with the slotted voltage reference plane/isolated signal traces embodiment of "figure 13"."

Applicants disagree with the Examiner's characterization that figure 11 and figure 13 necessarily represent different embodiments. In describing Fig. 13, the specification states at the second sentence of paragraph 0034 that "[a]s shown in Figure 13, a layer of conductive material on a **substrate** 32 has been removed only around the coplanar signal traces 38. Methods of removing selected portions of conductive material from a substrate, such as by masking and etching, are well known in the art."

Furthermore, in describing Fig. 11, the specification, prior to the amendment herein, states that "Figure 11 illustrates an embodiment of the present invention wherein circuit traces 24 are placed on the surface of a **semiconductor substrate** 26, more particularly, in a flip-chip ball grid array ("BGA") application. Like previous embodiments, the circuit traces 24 are configured such that a voltage reference trace is placed between each of two signal traces so that no signal trace is placed immediately adjacent another signal trace."

However, the specification generally refers to a substrate as a generic term encompassing different forms of substrate. For example, paragraph 0027 of the specification states "[a]s used herein, the term "circuit trace" refers not only to a surface conductive path which is conventionally formed upon the surface of a printed circuit board, but to any conductive path formed on, in or through **a substrate such as a printed circuit board, thin film device or other semiconductor device**." Similarly, at paragraph 0035, the specification states that "[f]igure 14 is a block diagram of an electronic system 100 which includes components having one or more **printed circuit boards ("PCB") 106 or other substrates** comprising circuit traces configured according to one or more embodiments of the present invention." Finally, at paragraph 0036, the specification states that "[a]s shown in Figure 15, **circuit traces 118 may be fabricated on the surface of a semiconductor wafer** 116 of silicon, gallium arsenide, or indium phosphide in accordance with one or more embodiments of the present invention."

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The specification, in its discussion of Fig. 13 describes a "substrate." It is clear, therefore, that the embodiment illustrated in Fig. 13 may be applied to any of the recited substrates, and their equivalents. Therefore, Fig. 13, and the description of Fig. 13 is applicable to the embodiment of Fig. 11 including solder balls and a semiconductor substrate as is found in a ball grid array.

Claims 28 through 30, stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

The Examiner states that:

> "it is unclear whether the recited "electrically insulative layer" can properly depend from or properly further limit a "substrate" which has been previously defined as being a "semiconductor". That is to say, a "semiconductor" has material properties which are materially different from that of "an electrically insulative layer" and as such would appear incompatible with it's use as a "semiconductor substrate." Clarification is needed."

In clarification, Applicant points out that a portion of claim 28 recites "wherein the semiconductor substrate includes: an electrically insulative layer **disposed on** the electrically conductive layer; and an additional electrically conductive layer disposed on the electrically insulative layer." As a consequence, the electrically insulative layer is not necessarily part of the "bare" semiconductor substrate, as the Examiner seems to be implying. Rather, the electrically insulative layer is **disposed on** the semiconductor substrate, with a material such as an oxide or passivation layer, to create a semiconductor substrate with multiple routing layers as is commonly know by those of ordinary skill in the art.

Claims 29 and 30 depend from claim 28 and, therefore, include the same element of "an electrically insulative layer **disposed on** the electrically conductive layer."

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,181,278 to Kakimoto et al. in view of U.S. Patent No. 5,796,321 to Caillat et al.

Claims 24 and 26, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kakimoto et al. (U.S. Patent No. 6,181,278) in view of Caillat et al. (U.S. Patent No. 5,796,321). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Regarding claim 24, in rejecting claim 24 the Examiner states, in part, that:

> "Kakimoto et al discloses in fig. 21 thereof, a ground and signal trace pattern configuration disposed on a surface of a semiconductor substrate (20). Note that the pattern comprises a voltage reference or ground plane (210) substantially surrounding the surface of the semiconductor substrate and patterned to include slots therein."

However, the Examiner has not addressed the element as recited in claim 24 of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots." Even if one considers the conductive trace connected to element 37a in FIG. 21 a signal trace, which is not entirely clear from the figure or the detailed description, there is not a voltage reference plane that provides a **continuous electrical connection** around the conductive trace connected to element 37a. Rather, there appears to be eight different segments surrounding most of the conductive trace connected to element 37a. Therefore, these eight different segments, by themselves do not form a voltage reference plane

that provides a **continuous electrical connection** around the conductive trace, as is recited in claim 24. Instead, it appears to Applicant, that these eight different segments are separate conductive traces of a possible voltage reference plane, if they are connected together.

Applicant recognizes that in discussing FIG. 21, Kakimoto et al. apparently describe external methods of connecting these eight different segments together to "attain a same potential" (col. 13, line 44). However, this requires additional elements, not recited in claim 24, to operably couple the eight different segments together.

Furthermore, Applicant can find no teaching or suggestion in the Caillat reference to the element of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots," as is recited in claim 24.

Therefore, Applicant asserts that the 35 U.S.C. § 103(a) rejection of claim 24 is improper because the element of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots," is not taught or suggested by the combination of Kakimoto et al. in view of Caillat et al. As a result, Applicant respectfully requests that the rejection of claim 24 be withdrawn.

Regarding claim 26, Applicant submits that claim 26 is allowable, at least by virtue of its dependency from allowable base claim 24. Applicant, therefore, respectfully requests reconsideration and allowance of claim 26.

Obviousness Rejection Based on U.S. Patent No. 6,175,287 to Lampen et al in view of U.S. Patent No. 5,796,321 to Caillat et al.

Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lampen et al. (U.S. Patent No. 6,175,287) in view of Caillat et al. (U.S. Patent No. 5,796,321). Applicant respectfully traverses this rejection, as hereinafter set forth.

Regarding claim 24, in rejecting claim 24 the Examiner states, in part, that:

> "Lampen et al in fig. 6 discloses a semiconductive MMIC having a ground or voltage reference plane (68) disposed over substantially the entire surface of the MMIC. Moreover, note that the ground plane includes a plurality of slots (72)

disposed therein in which respective short conductive traces or pads (70) are disposed. Furthermore, note that the traces are disposed such that the ground plane electrically isolates adjacent conductive traces."

However, as with the rejection discussed above concerning Kakimoto et al., the Examiner has not addressed the element as recited in claim 24 of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots." FIG. 6 of the Lampen reference does not show, nor can Applicants find any description in the specification of the ground plane 68 forming a continuous electrical connection around the conductive traces or pads (70).

Furthermore, Applicant can find no teaching or suggestion in the Caillat reference to the element of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots," as is recited in claim 24.

Therefore, Applicant asserts that the 35 U.S.C. § 103(a) rejection of claim 24 is improper because the element of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots," is not taught or suggested by the combination of Lampen et al. in view of Caillat et al. As a result, Applicant respectfully requests that the rejection of claim 24 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 6,181,278 to Kakimoto et al. and/or U.S. Patent No. 6,175,287 to Lampen et al. in view of U.S. Patent No. 5,796,321 to Caillat et al. and further in view of U.S. Patent No. 5,631,446 to Quan

Claim 25, stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kakimoto et al. (U.S. Patent No. 6,181,278) and/or Lampen et al. (U.S. Patent No. 6,175,287) in view of Caillat et al. (U.S. Patent No. 5,796,321), and further in view of Quan (U.S. Patent No. 5,631,446). Applicant respectfully traverses this rejection, as hereinafter set forth.

Regarding claim 25, Applicant submits that claim 25 is allowable, at least by virtue of its dependency from allowable base claim 24. Applicant, therefore, respectfully requests reconsideration and allowance of claim 25.

Obviousness Rejection Based on U.S. Patent No. 6,373,740 to Forbes et al. in view of either U.S Patent No. 6,181,278 to Kakimoto et al., U.S. Patent No. 6,232,660 to Kakimoto et al. or U.S. Patent No. 6,175,287 to Lampen et al., as modified by U.S. Patent No. 5,796,321 to Caillat et al.

Claim 31 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Forbes (U.S. Patent No. 6,373,740) in view of either Kakimoto et al. (U.S. Patent No. 6,232,660), Kakimoto et al. (U.S. Patent No. 6,175,287), or Lampen et al. (U.S. Patent No. 6,175,287), as modified by Caillat et al. (U.S. Patent No. 5,796,321). Applicant respectfully traverses this rejection, as hereinafter set forth.

Regarding claim 31, claim 31 includes all of the subject matter of independent claim 24. Therefore, the analysis presented above for the obviousness rejection of claim 24 with respect to Kakimoto et al. ('278) in view of Caillat et al. and the obviousness rejection of claim 24 with respect to Lampen et al. in view of Caillat et al. are equally applicable to claim 31.

In addition, as stated by the Examiner, "Forbes discloses an electronic system including a processor, memory device, input device, output device, data storage device, etc, but does not disclose such devices being semiconductor substrates having the recited conductive patterns connected by solder balls." Finally, Applicant can find no description in the Kakimoto et al.'660 reference of the element recited in claim 31 of, "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots."

Therefore, Applicant asserts that the 35 U.S.C. § 103(a) rejection of claim 31 is improper because the element of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots," is not taught or suggested by the combination of Forbes et al. in view of either Kakimoto et al. '660 or Kakimoto et al. '287 or Lampen et al., as modified by Caillat et al. As a result, Applicant respectfully requests that the rejection of claim 31 be withdrawn.

ENTRY OF AMENDMENTS

The amendments to the specification and drawings above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 24-26 and 28-31 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,

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Registration No. 50,978
Attorney for Applicant
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: April 4, 2006
JMM/sfc:eg
Document in ProLaw

APPENDIX

(REPLACEMENT SHEET AND ANNOTATED SHEET SHOWING CHANGES)

(Serial No. 09/548,942)

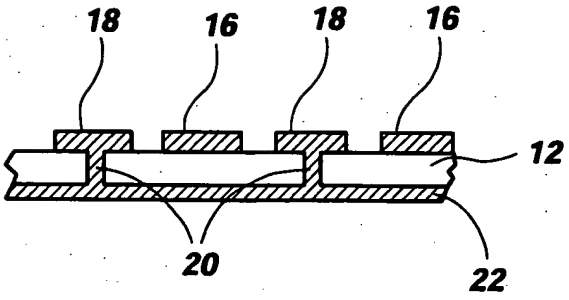

Fig. 6

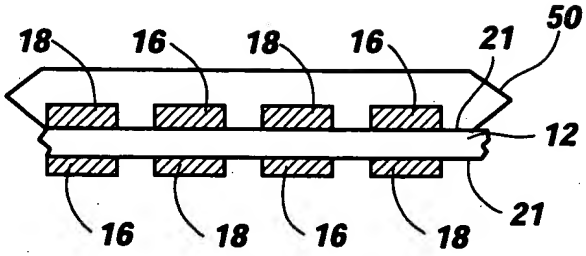

Fig. 8

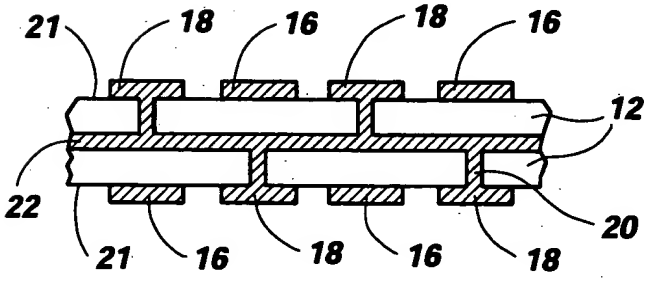

Fig. 7

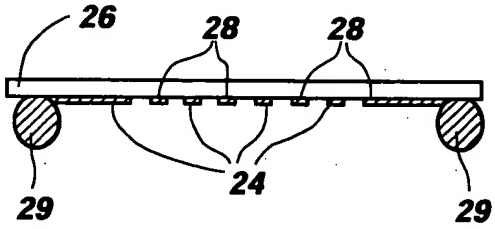

Fig. 11

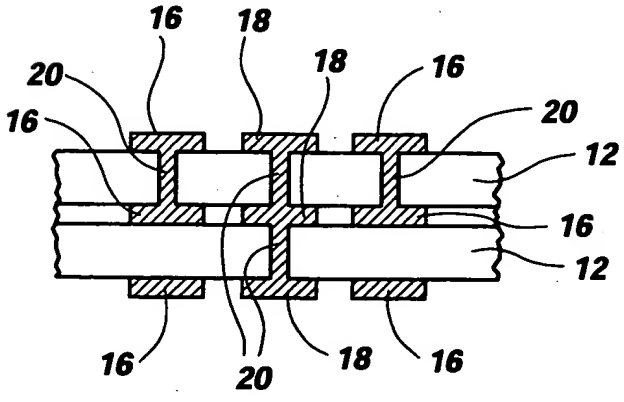

Fig. 10

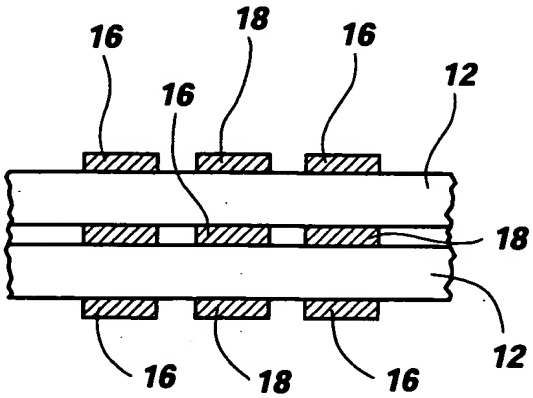

Fig. 9

TITLE: METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES
Serial No.: 09/548,942
Docket No.: 2269-4161US
ANNOTATED SHEET SHOWING CHANGES

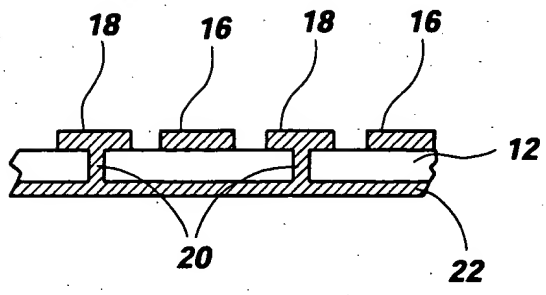

Fig. 6

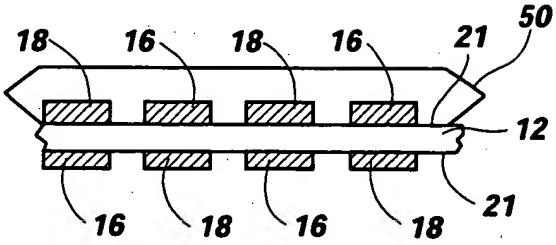

Fig. 8

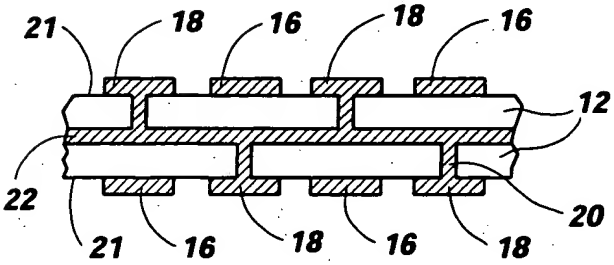

Fig. 7

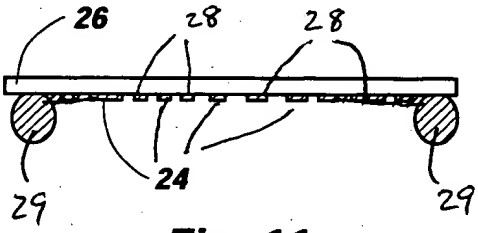

Fig. 11

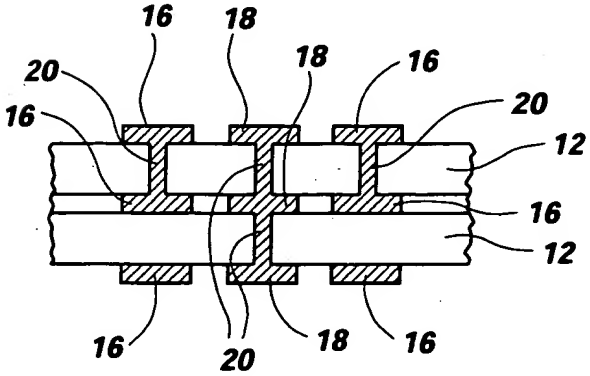

Fig. 10

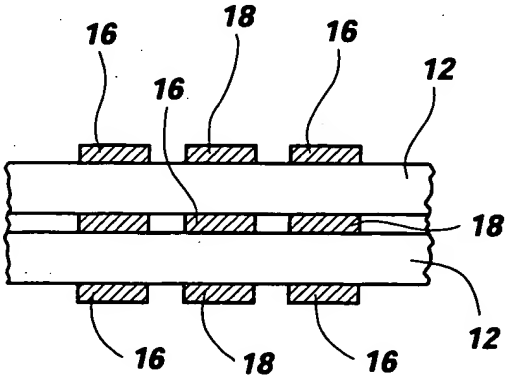

Fig. 9

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